19-2560; Rev 0; 7/02

EVALUATION KIT AVAILABLE

MAXIM

Low-Voltage, Low-Dropout Linear Regulators with External Bias Supply

General Description

The MAX1982/MAX1983 are low-voltage, low-dropout linear regulators with an external bias supply input. The 5V bias supply drives the gate of the internal N-channel pass transistor, making these devices ideal for applications that require low-voltage outputs from low-voltage inputs. The MAX1982 delivers 1.2V (±3%) at 300mA from an input voltage of 1.25V to 5.5V. The MAX1983 delivers an adjustable output voltage from 0.8V to 2V.

The MAX1982/MAX1983 include a current-limit and thermal shutdown that protects the regulator in the event of a fault condition. Both devices are offered in a 6-pin SOT23 package and are specified over the extended (-40°C to +85°C) temperature range.

Applications

Notebook Computers

VID Power Supplies

PDAs

Cell Phones

Low-Dropout Regulators with External Bias Supply

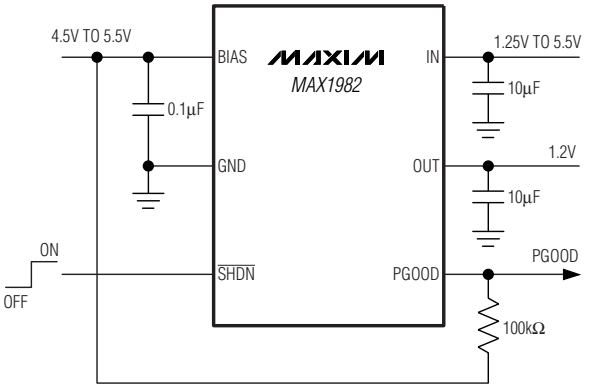
Features

- **Low-Cost 1.2V, 300mA VID Supply**
- **±3% Output Voltage Accuracy**
- **No Minimum Load Current Required**
- **1.25V to 5.5V Input Supply Voltage**
- **5V Input Bias Supply Voltage**
- **Power-Good (PGOOD) Open-Drain Output with 1ms Rising Edge Propagation Delay (MAX1982)**
- **Adjustable Output Voltage (MAX1983)**
- **Low Supply Current (I_{BIAS} + I_{IN} = 165µA typ)**
- **5µA (max) Shutdown Supply Current**
- **Tiny 6-Pin SOT23 Package**

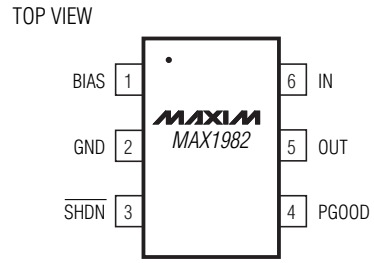
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX1982EUT-T	-40°C to +85°C	6 SOT23-6	ABEA
MAX1983EUT-T	-40°C to +85°C	6 SOT23-6	ABEB

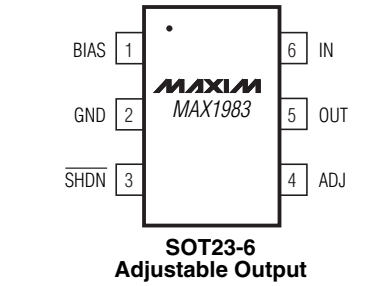
Typical Operating Circuit



Pin Configurations



SOT23-6
Fixed Output Voltage



SOT23-6
Adjustable Output

Low-Voltage, Low-Dropout Linear Regulators with External Bias Supply

ABSOLUTE MAXIMUM RATINGS

ADJ, IN, BIAS, PGOOD, $\overline{SHDN}$, OUT to GND.....-0.3V to +6V
Output Short-Circuit Duration .....Infinite
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 3, V_{IN} = 1.8V, I_{LOAD} = 1mA, C_{LOAD} = 10µF, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}		1.25		5.5	V
BIAS Voltage	V_{BIAS}		4.5		5.5	V
V_{OUT} Voltage Range	V_{OUT}	MAX1983	0.8		2.0	V
BIAS Input Undervoltage Lockout			3.8	4.1	4.35	V
Shutdown Supply Current	I_{IN}	1.25V < V_{IN} < 5.5V		1	5	µA
Quiescent BIAS Current	I_Q	4.5V < V_{BIAS} < 5.5V		140	250	µA
Shutdown BIAS Current	$I_{\overline{SHDN}}$	4.5V < V_{BIAS} < 5.5V		1	5	µA
V_{OUT} Input Bias Current		MAX1982: V_{IN} = open, V_{OUT} = 1.20V			30	µA
		MAX1983: V_{IN} = open, 0.8V < V_{OUT} < 2.0V			2	
MAX1983 ADJ Input Current		0V < V_{ADJ} < 2.0V			1	µA
REGULATOR CHARACTERISTICS						
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	I_{LOAD} = 10mA, 1.5V < V_{IN} < 5.5V	-0.15		+0.15	%/V
MAX1982 1.20V Output Voltage Accuracy	V_{OUT}	T_A = +25°C, I_{OUT} = 100mA	-1		+1	%
		T_A = 0°C to +85°C, I_{OUT} = 1mA to 300mA, V_{OUT} + 0.5V < V_{IN} < 5.5V	-3		+3	
MAX1983 0.80V Output Voltage Accuracy	V_{OUT}	T_A = +25°C, I_{OUT} = 100mA	-1		+1	%
		T_A = 0°C to +85°C, I_{OUT} = 1mA to 300mA, V_{OUT} + 0.5V < V_{IN} < 5.5V	-3		+3	
Dropout Voltage	V_{DO}	I_{LOAD} = 300mA			350	mV
		I_{LOAD} = 150mA			175	
Current Limit	I_{LIM}	V_{IN} - V_{OUT} = 1.3V	330	600	1400	mA
Thermal-Shutdown Temperature	$T_{\overline{SHDN}}$			160		°C
Thermal-Shutdown Hysteresis				20		°C
RMS Output Noise		10Hz to 100kHz		65		μV_{RMS}
PGOOD COMPARATOR						
Comparator Threshold		% of regulated output voltage	-12.5	-9	-6	%
Comparator Hysteresis	V_{HYST}			10		mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 3, V_{IN} = 1.8V, I_{LOAD} = 1mA, C_{LOAD} = 10µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC AND I/O						
$\overline{SHDN}$ Input High Voltage	V_{IH}		2.4			V
$\overline{SHDN}$ Input Low Voltage	V_{IL}				0.8	V
$\overline{SHDN}$ Input Current			-1		+1	µA
PGOOD Output Low Voltage		PGOOD sinking 1mA			0.1	V
PGOOD Output High Leakage Current		$0 < V_{PGOOD} < V_{IN}$	-1		+1	µA
DYNAMICS						
Positive Load Step	t_{RISE}	I_{LOAD} = 1mA to full load, C_{LOAD} = 10µF		10		µs
Negative Load Step	t_{FALL}	I_{LOAD} = full load to 1mA, C_{LOAD} = 10µF		50		µs
Ripple Rejection at V_{IN}		10Hz < f < 10kHz, I_{LOAD} = 300mA, C_{LOAD} = 10µF		-60		dB
Startup Response Time	t_{ON}	I_{LOAD} = 300mA, C_{LOAD} = 10µF, 0% to 90% of nominal output voltage		100		µs
Startup Overshoot		I_{LOAD} = 300mA, C_{LOAD} = 10µF		0.5		%
PGOOD Propagation Delay	t_{PD}	Falling edge, 3mV under trip threshold		10		µs
		Rising edge within 5% of regulation level	1		4	ms

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 3, V_{IN} = 1.8V, I_{LOAD} = 1mA, C_{LOAD} = 10µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Voltage	V_{IN}		1.25	5.5	V
BIAS Voltage	V_{BIAS}		4.5	5.5	V
V_{OUT} Voltage Range	V_{OUT}	MAX1983	0.8	2.0	V
BIAS Input Undervoltage Lockout			3.8	4.2	V
Shutdown Supply Current	I_{IN}	1.25V < V_{IN} < 5.5V		5	µA
Quiescent BIAS Current	I_Q	4.5V < V_{BIAS} < 5.5V		250	µA
Shutdown BIAS Current	$I_{\overline{SHDN}}$	4.5V < V_{BIAS} < 5.5V		5	µA
V_{OUT} Input Bias Current		MAX1982: V_{IN} = open, V_{OUT} = 1.20V		30	µA
		MAX1983: V_{IN} = open, 0.8V < V_{OUT} < 2.0V		2	
REGULATOR CHARACTERISTICS					
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	I_{LOAD} = 10mA, 1.5V < V_{IN} < 5.5V	-0.15	+0.15	%/V
MAX1982 1.20V Output Voltage Accuracy	V_{OUT}	I_{OUT} = 1mA to 300mA, V_{OUT} + 0.5V < V_{IN} < 5.5V	-3	+3	%

Low-Voltage, Low-Dropout Linear Regulators with External Bias Supply

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 3, V_{IN} = 1.8V, V_{OUT} = 1.2V, I_{LOAD} = 1mA, C_{LOAD} = 10µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

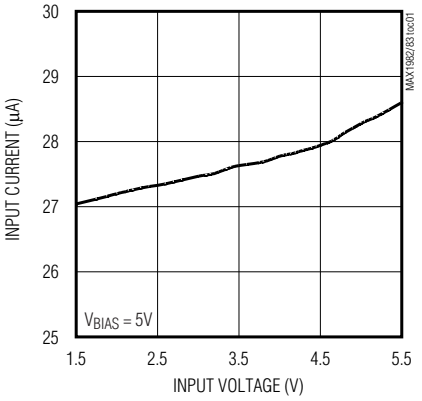
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
MAX1983 0.80V Output Voltage Accuracy	V_{OUT}	I_{OUT} = 1mA to 300mA, V_{OUT} + 0.5V < V_{IN} < 5.5V	-3	+3	%
Dropout Voltage	V_{DO}	I_{LOAD} = 300mA		350	mV
		I_{LOAD} = 150mA		175	
Current Limit	I_{LIM}	V_{IN} - V_{OUT} = 1.3V	330	1400	mA
PGOOD COMPARATOR					
Comparator Threshold		% of regulated output voltage	-12.5	-6	%
LOGIC AND I/O					
$\overline{SHDN}$ Input High Voltage	V_{IH}		2.4		V
$\overline{SHDN}$ Input Low Voltage	V_{IL}			0.8	V
$\overline{SHDN}$ Input Current			-1	+1	µA
PGOOD Output Low Voltage		PGOOD sinking 1mA		0.1	V
PGOOD Output High Leakage Current		0 < V_{PGOOD} < V_{IN}	-1	+1	µA
DYNAMICS					
PGOOD Propagation Delay	t_{PD}	Rising edge within 5% of regulation level	1	4	ms

Note 1: Specifications over temperature are guaranteed by design, not production tested.
Note 2: V_{OUT} is 1.2V for MAX1982. For MAX1983 V_{OUT} is set to 1.2V with circuit of Figure 4.

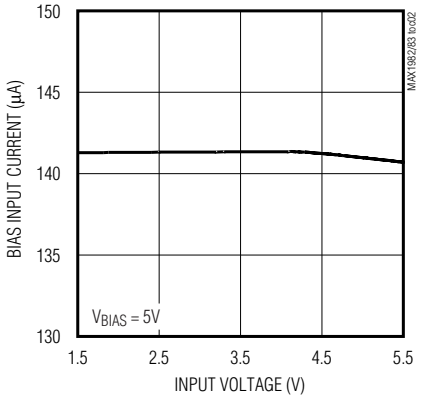
Typical Operating Characteristics

(Circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

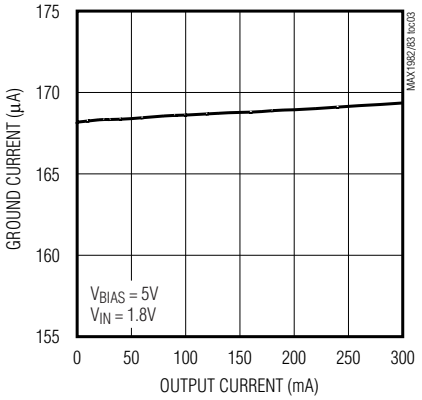
INPUT CURRENT vs. INPUT VOLTAGE



BIAS INPUT CURRENT vs. INPUT VOLTAGE



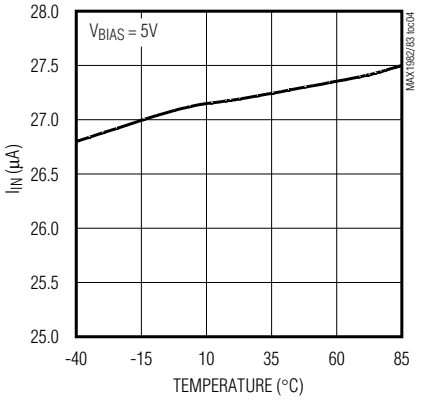
GROUND CURRENT vs. OUTPUT CURRENT



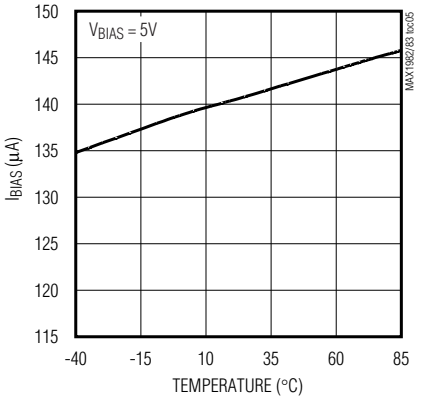
Typical Operating Characteristics (continued)

(Circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

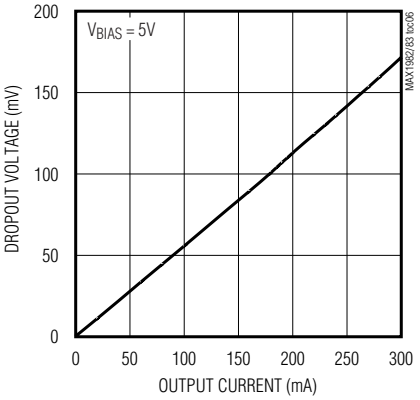
INPUT CURRENT vs. TEMPERATURE



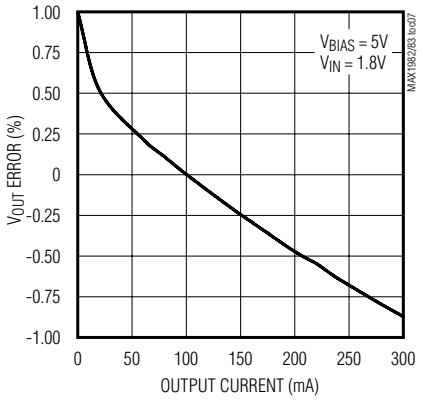
BIAS SUPPLY CURRENT vs. TEMPERATURE



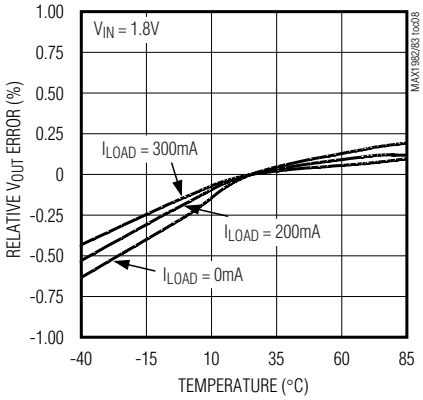
DROPOUT VOLTAGE vs. OUTPUT CURRENT



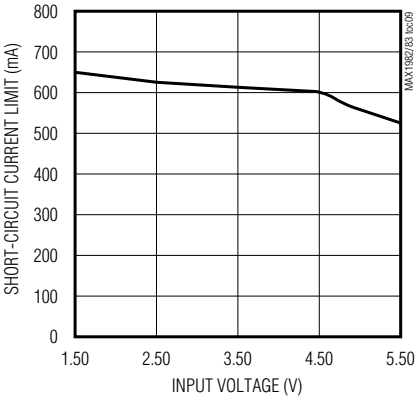
OUTPUT VOLTAGE ERROR vs. OUTPUT CURRENT



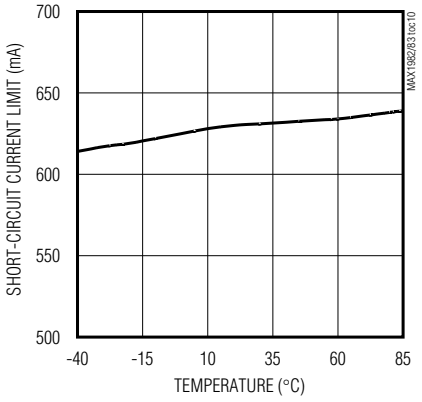
OUTPUT VOLTAGE ERROR vs. TEMPERATURE



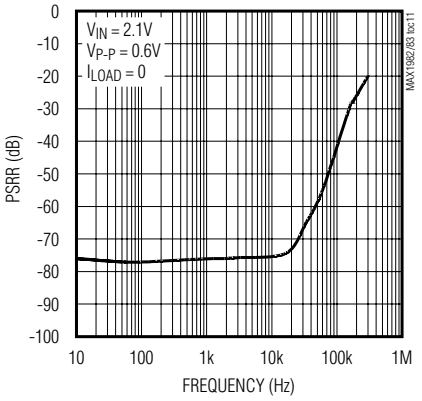
SHORT-CIRCUIT CURRENT LIMIT vs. INPUT VOLTAGE



SHORT-CIRCUIT CURRENT LIMIT vs. TEMPERATURE



POWER-SUPPLY REJECTION RATIO (V_{IN}) vs. FREQUENCY

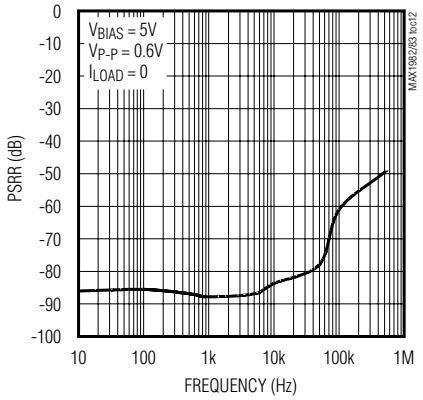


Low-Voltage, Low-Dropout Linear Regulators with External Bias Supply

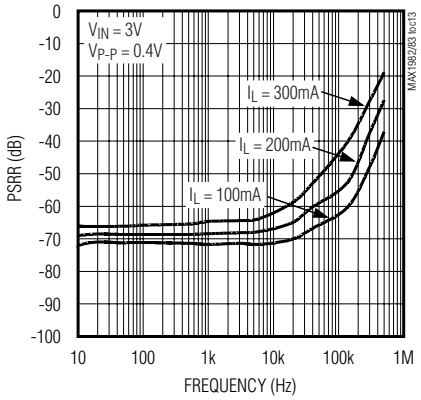
Typical Operating Characteristics (continued)

(Circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

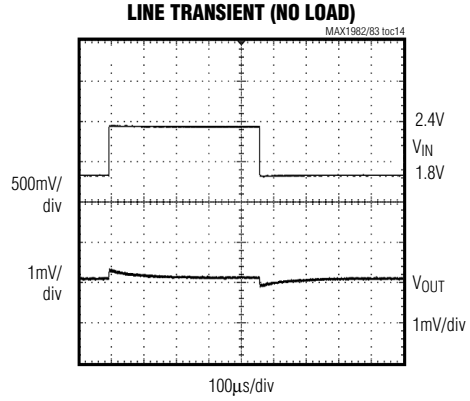
POWER-SUPPLY REJECTION RATIO (V_{BIAS}) vs. FREQUENCY



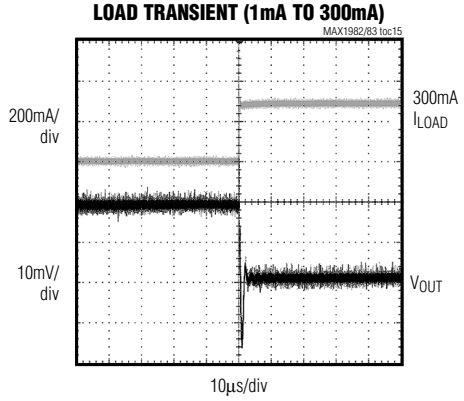
RIPPLE REJECTION RATIO (V_{IN}) vs. FREQUENCY



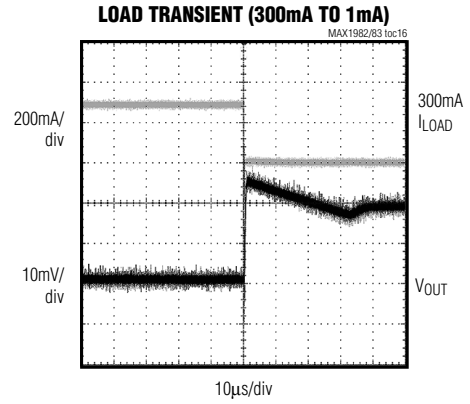
LINE TRANSIENT (NO LOAD)



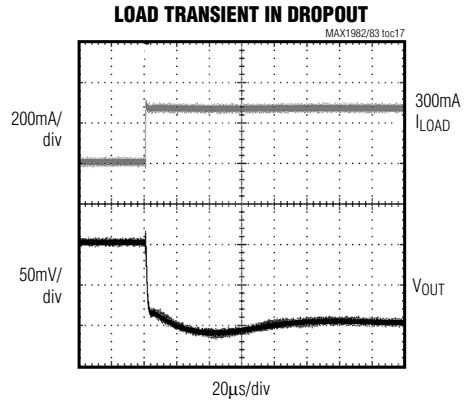
LOAD TRANSIENT (1mA TO 300mA)



LOAD TRANSIENT (300mA TO 1mA)



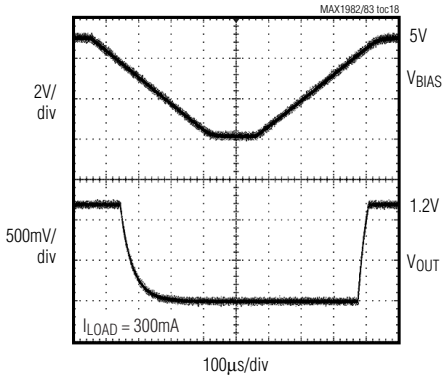
LOAD TRANSIENT IN DROPOUT



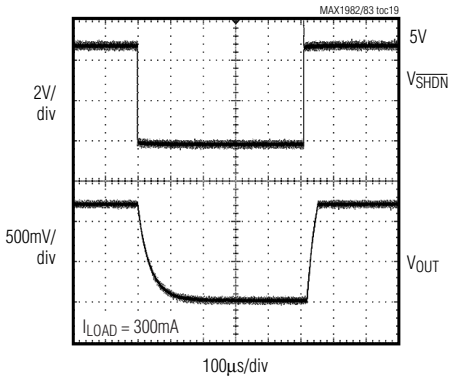
Typical Operating Characteristics (continued)

(Circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

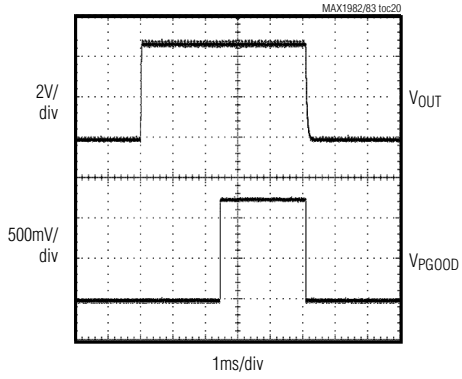
UNDERVOLTAGE LOCKOUT



SHUTDOWN RESPONSE



PGOOD RESPONSE



Low-Voltage, Low-Dropout Linear Regulators with External Bias Supply

Pin Description

PIN		NAME	FUNCTION
MAX1982	MAX1983		
1	1	BIAS	Bias Voltage. Input voltage to the control circuitry. BIAS powers all control blocks and the gate of the pass transistor. Bypass BIAS to GND with a 0.1µF ceramic capacitor.
2	2	GND	Ground
3	3	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to enter the low-power shutdown state. Connect $\overline{SHDN}$ to BIAS for normal operation.
4	—	PGOOD	Power-Good Output. The open-drain PGOOD output goes high at least 1ms after the output voltage has attained regulation. PGOOD asserts low 10µs after the output falls by 10%.
—	4	ADJ	Feedback for Adjustable Output. Connect ADJ to the midpoint of a resistor-divider between OUT and GND for an adjustable output voltage between 0.8V and 2.0V.
5	5	OUT	Regulator Output. Bypass OUT to GND with a 10µF to 22µF low-ESR ceramic capacitor.
6	6	IN	Internal Pass Transistor Input. IN connects to the drain of the internal power switch. Bypass IN to GND with a 10µF ceramic capacitor.

Detailed Description

The MAX1982/MAX1983 are low-voltage, low-dropout linear regulators with an external bias supply input (see Figures 1 and 2). BIAS is powered by a 4.5V to 5.5V supply that is commonly available in laptop and desktop computers. The 5V bias supply drives the gate of the internal pass transistor, while a lower voltage input at the drain of the transistor (IN) is regulated to provide V_{OUT}. Separating the bias input voltages yields higher efficiency. These devices are ideal for applications that require low-voltage outputs from low-voltage inputs. The MAX1982 delivers 1.2V (±3%) at 300mA from an input voltage of 1.25V to 5.5V. The MAX1983 delivers an adjustable output voltage from 0.8V to 2V.

The MAX1982 features an open-drain PGOOD output that transitions high 1ms after the output reaches regulation. PGOOD goes low within 10µs of the output falling out of regulation by 120mV.

Both devices feature current- and thermal-limiting circuitry that protect the MAX1982/MAX1983 from damage during fault conditions.

Bias Supply Input

The BIAS input powers the control circuitry and provides the pass transistor gate drive. Power BIAS from a well-regulated 5V (±10%) supply. Current drawn from the BIAS supply remains relatively constant with variations in V_{IN} and load current (see the *Typical Operating Characteristics*). Bypass BIAS with a 0.1µF or greater capacitor as close to the device as possible. The bias supply current remains low (250µA) when the MAX1982/MAX1983 are in dropout.

Power-Supply Input

IN connects to the drain of the internal N-channel power transistor. IN may be as low as 1.25V, minimizing power dissipation. Bypass IN with a 10µF or greater capacitor as close to the device as possible.

Shutdown

The MAX1982/MAX1983 feature a low-power shutdown mode that reduces quiescent current drawn to 1µA (typ), and BIAS current consumption to less than 1µA (typ). Driving $\overline{SHDN}$ low disables the voltage reference, error amplifier, gate-drive circuitry, and pass transistor (see Figure 2), and the device output enters a high-impedance state. Connect $\overline{SHDN}$ to BIAS for normal operation.

PGOOD Output

The MAX1982 provides an open-drain PGOOD output that goes high 1ms (min) after the output attains regulation (within 10% of the nominal output voltage). PGOOD transitions low 10µs after the output falls out of regulation by 120mV, or when the device enters shutdown. Connect a pullup resistor from PGOOD to BIAS for a logic-level output. Use a 100kΩ resistor to minimize current consumption.

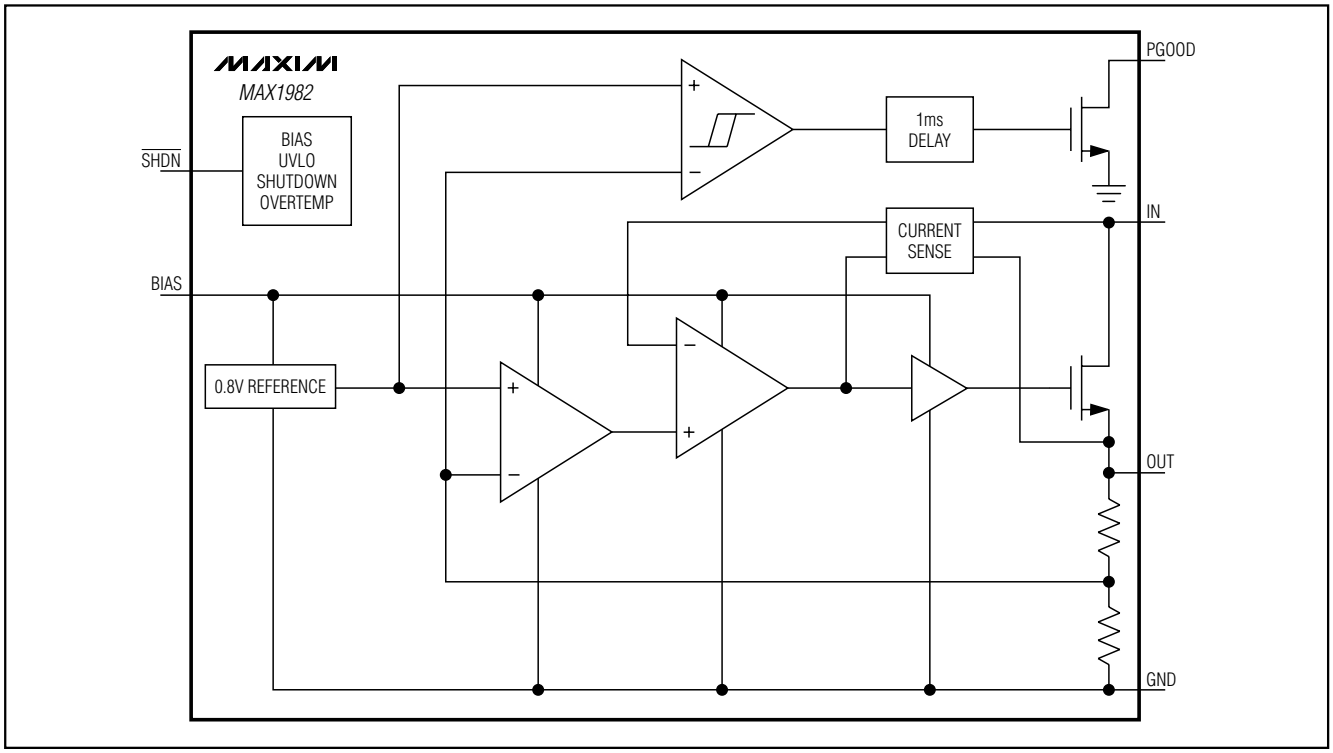


Figure 1. MAX1982 Functional Diagram

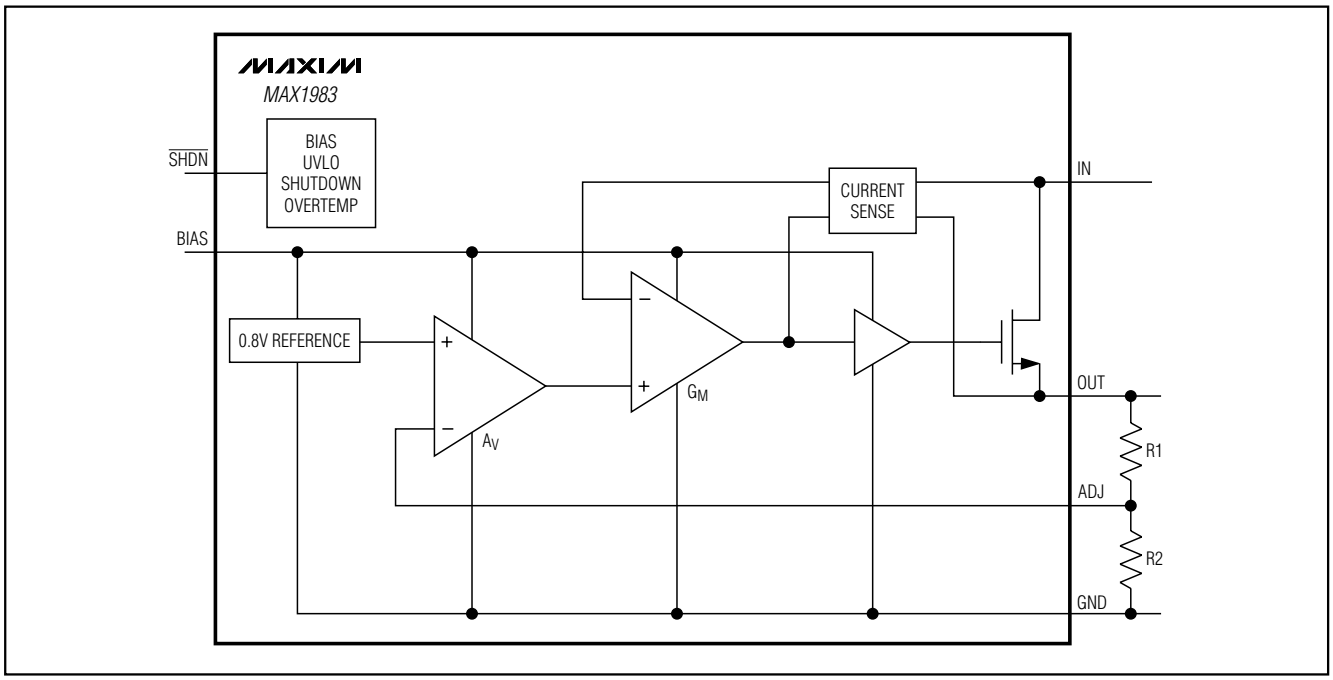


Figure 2. MAX1983 Functional Diagram

Low-Voltage, Low-Dropout Linear Regulators with External Bias Supply

Current Limit

The MAX1982/MAX1983 limit the output current to 600mA (typ) in the event of an overload or output short circuit. The current limit prevents damage to the internal power transistor, but the device can enter thermal shutdown if the power dissipation is great enough to increase the die temperature above +160°C (see the *Thermal-Overload Protection* section).

Thermal-Overload Protection

Thermal-overload protection limits the power dissipation in the MAX1982/MAX1983. When the die temperature exceeds +160°C, the pass transistor turns off, allowing the device to cool. Normal operation resumes when the die temperature cools by 20°C. A continuous thermal-overload condition results in a pulsed output. For continuous operation, do not exceed a junction temperature of +150°C.

Applications Information

Output Voltage Selection

The MAX1982 output is fixed at 1.2V. The MAX1983 provides an adjustable output (0.8V to 2.0V). Connect ADJ to a resistive voltage-divider between OUT and GND as shown in Figure 4. Set the output voltage using the following equation:

$$V_{OUT} = 0.8V\left(1+\frac{R1}{R2}\right)$$

Set R2 at 40kΩ and choose R1 to achieve the desired output voltage. Set V_{IN} to higher than (V_{OUT} + 400mV) to meet the dropout voltage requirement (see the *Input/Output (Dropout) Voltage* section).

To ensure stability over the specified input voltage range, the minimum output capacitance must be 10µF with a maximum ESR of 35mΩ.

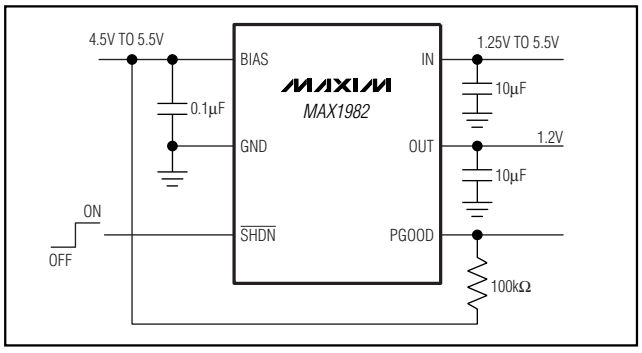


Figure 3. MAX1982 Typical Application Circuit

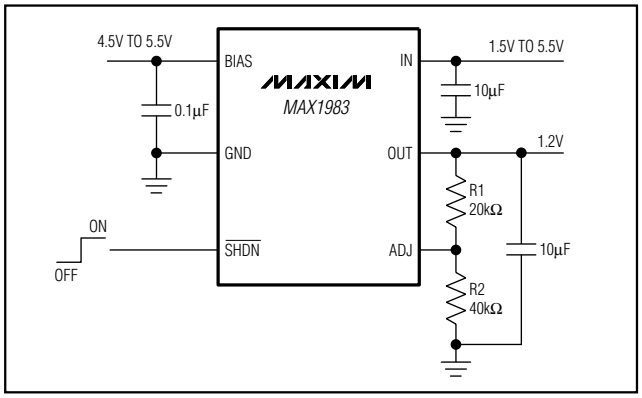


Figure 4. MAX1983 Typical Application Circuit

Operating Region and Power Dissipation

The maximum power dissipation of the MAX1982/MAX1983 depends on the thermal resistance of the 6-pin SOT23 package and the circuit board, the temperature difference between the die and ambient air, and the rate of airflow. The power dissipated in the device is:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT})$$

The resulting maximum power dissipation is:

$$P_{DISS(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature (+150°C) and T_A is the ambient temperature, θ_{JC} is the thermal resistance from the die junction to the package case, and θ_{CA} is the thermal resistance from the case through the PC board, copper traces, and other materials to the surrounding air. For optimum power dissipation, use a large ground plane with good thermal contact to GND, and use wide input and output traces.

When 1 square inch of copper is connected to the device, the maximum allowable power dissipation of a 6-pin SOT23 package is 696mW. The maximum power dissipation is derated by 8.7mW/°C above T_A = +70°C. Extra copper on the PC board increases thermal mass, and reduces thermal resistance of the board. Refer to the MAX1982/MAX1983 EV kit for a layout example.

The MAX1982/MAX1983 deliver up to 300mA and operate with input voltages up to 5.5V, but not simultaneously. High output currents can only be achieved when the input-output differential voltages are low (Figure 5).

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit ensures that the regulator starts up with adequate voltage for the gate-drive circuitry to bias the internal pass transistor.

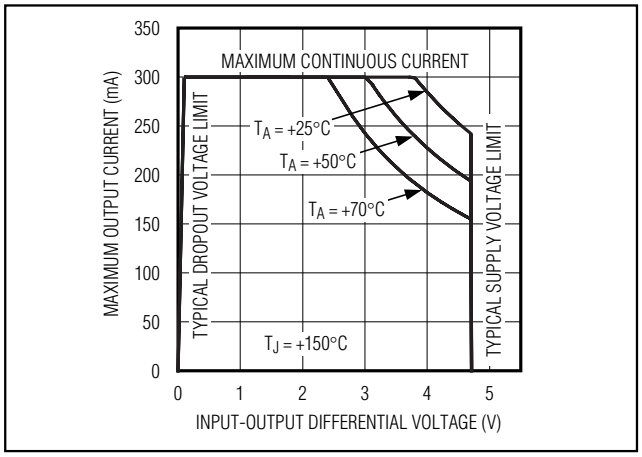


Figure 5. Power Operating Region—Maximum Output Current vs. Supply Voltage

The UVLO circuitry monitors V_{BIAS} only. The UVLO threshold is 4.2V, and V_{BIAS} must remain above this level for proper operation, regardless of the level of V_{IN}.

Input Capacitor

Bypass IN to ground with a 10µF or greater ceramic capacitor. Bypass BIAS to ground with a 0.1µF ceramic capacitor for normal operation in most applications.

Output Capacitor

Bypass OUT to ground with a low-ESR ceramic capacitor greater than 10µF. The ESR must be less than 35mΩ. Choose an output capacitor to maintain the required output voltage tolerance during a load step. The change in output voltage is,

$$\Delta V = I\left[ESR + \frac{\Delta t}{C_{OUT}}\right]$$

where I is the load current, C_{OUT} is the output capacitance, and Δt is the duration of the load step.

Noise, PSRR, and Transient Response

The MAX1982/MAX1983 operate with low-dropout voltage and low quiescent current in notebook computers while maintaining good noise, transient response, and AC rejection specifications. See the *Typical Operating Characteristics* for a graph of Power-Supply Rejection Ratio (PSRR) vs. Frequency. Improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output capacitors and use passive filtering techniques when operating from noisy sources.

The MAX1982/MAX1983 load-transient response graphs (see the *Typical Operating Characteristics*) show two components of the output response: a DC shift from the output impedance due to the load current change and the transient response. A typical transient response for a step change in the load current from 1mA to 300mA is 20mV. Increasing the output capacitor's value and decreasing the ESR attenuate the overshoot.

Input/Output (Dropout) Voltage

A regulator's minimum input-to-output voltage differential (dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, the dropout voltage determines the useful end-of-life battery voltage. Because the MAX1982/MAX1983 use an N-channel pass transistor, the dropout voltage is a function of the drain-to-source on-resistance ($R_{DS(ON)}$ = 1Ω max) multiplied by the load current (see the *Typical Operating Characteristics*):

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

PC Board Layout Guidelines

The MAX1982/MAX1983 require proper layout to achieve the intended output power level, high efficiency, and low noise. Proper layout involves the use of a ground plane, appropriate component placement, and correct routing of traces using appropriate trace widths.

1) Minimize high-current ground loops. Connect the ground of the device, the input capacitor, and the output capacitor together at one point.
2) To optimize performance, a ground plane is essential. Use all available copper layers in applications where the device is located on a multilayer board.
3) Connect the input filter capacitor less than 10mm from IN. The connecting copper trace carries large currents and must be at least 2mm wide, preferably 5mm wide.
4) Use as much copper as necessary to increase the thermal resistance of the device. In general, more copper provides better heatsinking capabilities.

Chip Information

TRANSISTOR COUNT: 430

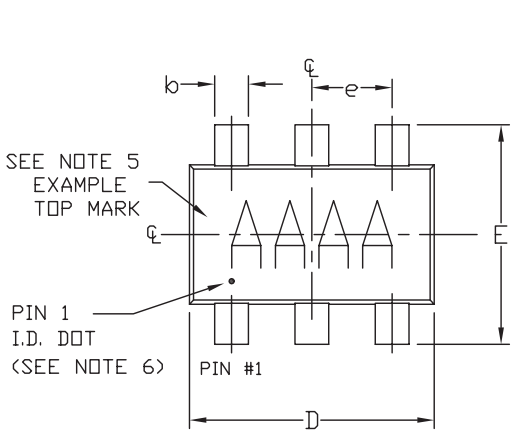
PROCESS: BiCMOS

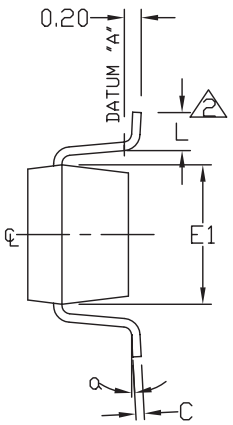
Low-Voltage, Low-Dropout Linear Regulators with External Bias Supply

Package Information

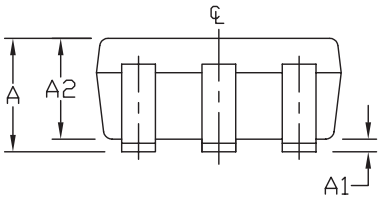
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6LSOT.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
α	0°	10°



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SOT-23, 6L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0058	E	1/1